REMARKS

This Amendment and Response is submitted in response to the Office Action mailed February 27, 2003, which has been received and carefully analyzed. Claims 1-5, and 22-23 have been cancelled. Claims 6-10, 12, 13, 15, and 24 have been amended.

Claims 1-5, and 22 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 3-4 and 10-11 of U.S Patent No. US 2002/0163059 A1. Applicants have cancelled those claims without prejudice from the present application for filing in a continuation application, thereby making the rejection moot.

Claims 6-9, 12, 15, and 23-24 were rejected under 35 U.S.C § 103(a) as being unpatentable over Blackstone et al. (U.S. Patent No. 5,164,813). Blackstone is directed to a low capacitance diode structure wherein there is a surface area reduction in the region of the bond of semi-conductor materials, resulting in an hour-glass-like cross section. See column 2, lines 34 - 40. Blackstone's structure describes and teaches a reduction of diode capacitance by creating a space between the unbonded edge regions of the constituent semi-conductor materials. This phenomenon is best illustrated in the drawing figures such as, Fig. 3D, 4D, and 4H-4K of Blackstone.

Furthermore, Blackstone is directed to the bonding of semi-conductor materials that are first patterned. The semi-conductor surfaces are patterned using mesa techniques, as described at column 2, lines 44 – 54. Blackstone's diode structure has a first semi-conductor layer (field – plate), which has a planar or mesa surface. The first semi-conductor layer is bonded to a second semi-conductor layer having a mesa surface. The resulting bonded structure has a half or full hourglass profile as shown in Fig. 4H, at the bond junction. A full hour-glass profile is produced

when the first semi-conductor layer has a mesa surface. Otherwise, a half hour-glass profile is produced for a planar surfaced first semi-conductor layer.

All of the described embodiments of Blackstone incorporate and require a certain amount of overhang of the diode junction by the field plates (semi-conductor layer). See column 7, lines 19-28 and column 7, lines 37 – 40. In the case of high voltage diodes, Blackstone's embodiment that is directed to high voltage applications comprises a multiplicity of field plates as shown in Fig. 11. See also column 7, lines 48-57.

Applicants' invention is neither taught nor suggested by Blackstone. Both the method for fabricating diodes and the structure of the diode devices in applicant's invention are quite distinct from the teachings or suggestions of Blackstone. Furthermore, Applicants' invention would not have been obvious in light of Blackstone. Applicants' inventive etching of either the substrate or epitaxial layer is not the same nor is it suggested or taught by the mesa based bonding of Blackstone. The diffusion or epitaxial growth of a conductive layer type within the etched area is also quite distinct and novel.

Blackstone teaches creating a mesa 128 by carving out portions of a semiconductor layer of one conductivity type to leave behind the mesa 128. The mesa 128, which protrudes above the recesses in the layer, provides a narrow region that presents a reduced surface area to which another semi-conductor layer of a second conductivity type can be bonded. When all the layers of the Blackstone semiconductor are in place, there are hollow pocket regions i.e. cavity 152, in which there is no contact between the opposed junction layers. See Fig. 6, (column 6, lines 54-65) and Figs 3B, 3C and 4C. Furthermore, Blackstone requires the creation of the mesa 128 prior to the bonding of the various conductive layers.

To the contrary, Applicants carve out portions of a semiconductor device of one conductivity type to create a well. The well is the receptacle for material (by deposition or diffusion) that forms a layer of a second conductivity type. The second conductivity type is introduced into the well by either diffusion or epitaxial deposits. There is no cavity between any of the layers in Applicants semiconductor device. The moats of Applicants' invention are created after the various layers have been formed. The moats define the perimeter of individual semiconductor devices and provide those semiconductors with a positive bevel angle. There is no overhang of each of the 'field plates' or in this case, conductive layers to create a capacitive full or half hourglass like cross-section.

There is no teaching or suggestion in Blackstone to form a central cavity or well for each individual semiconductor device, into which a conductive layer can be introduced. Further, Blackstone does not teach or suggest a reduced distance between the layers of opposite conductivity at the location of the well, to reduce the electric field in said portion of the semiconductor device.

In light of this and other reasons stated earlier, claims 6-9, 12, 15, and 24 of Applicants' invention are non-obvious in light of Blackstone. Applicants respectfully request that the Examiner withdraw the rejections to these claims.

Claims 10-11, and 13-14 were rejected under 35 U.S.C § 103(a) as being unpatentable over Blackstone et al. as applied to claims 6-9, 12, 15, and 23-24, and further in view of Hamerski (US 2002/063059). For at least the reasons stated earlier, these claims are non-obvious in light of Blackstone. Furthermore, as previously set forth, Hamerski at the time of the present invention was made, was under an obligation for assignment to the same owner of the

present Application. Hamerski cannot be the basis of a prior art rejection in light of the common ownership, under Section 103(a).

Applicants' therefore assert that based on the claim limitations as explained in the remarks contained herein, the application is in condition for allowance. Favorable action and allowance of the claims and entry of these remarks into the record is respectfully requested.

None of the cited references, either alone or in any combination thereof, disclose or suggest the novel features associated with the present invention.

CONCLUSION

Entry of the above amendment and remarks are respectfully requested.

In view of the foregoing, consideration and allowance of this application are earnestly solicited. Further, a Notice of Allowance appears to be in order and such is courteously solicited. If any issue regarding the allowability of this application could be readily resolved, or if other action could be taken to further advance this application such as an Examiner's amendment, or if the Examiner should have any questions regarding the present amendment, it is respectfully requested that the Examiner please telephone Applicants' undersigned attorney in this regard. Applicants' request for extension of time under 37 CFR 1.136(a) is enclosed herewith. Please charge the appropriate extension fee and any other fees that may be due to Deposit Account No. 11-0160.

Respectfully submitted,

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